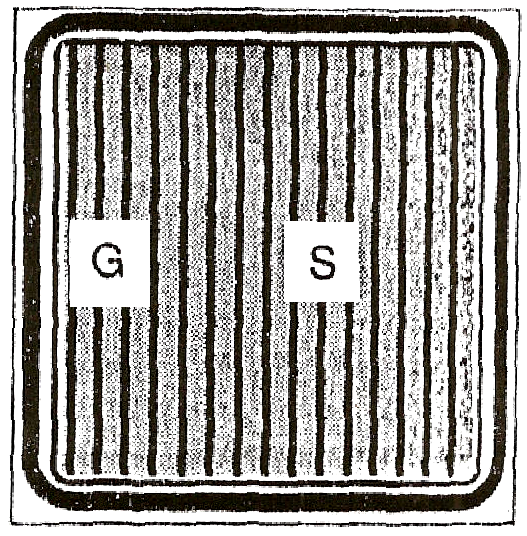
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.045”**



**.045”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .0064” X .0066”**

**Backside Potential: Drain**

**Mask Ref: VF25**

**APPROVED BY: DK DIE SIZE .045” X .045” DATE: 9/23/21**

**MFG: SUPERTEX THICKNESS .011” P/N: DN3525ND**

**DG 10.1.2**

#### Rev B, 7/19/02